**WHAT IS CLAIMED IS:**

1. An integrated circuit ("IC") simulation system operable to (i) store a plurality of Hardware Description Language ("HDL") modules, each one of said plurality of HDL modules representative of a circuit element, (ii) receive a HDL description of a circuit to be simulated, and (iii) synthesize a circuit netlist as a function of said received HDL circuit description and ones of said plurality of HDL modules, said circuit netlist defining behavioral relationships among associated ones of said ones of said plurality of HDL modules, and associate a timing-violation controller with said circuit netlist, said timing-violation controller to ignore selected timing violations sensed during simulation of said circuit as a function of ones of said defined behavioral relationships.

2. The IC simulation system as set forth in Claim 1 comprising a processor and associated memory.

3. The IC simulation system as set forth in Claim 2 wherein said associated memory is operable to store an IC-design process program and wherein said processor is operable to execute said IC-design process program.

4. The IC simulation system as set forth in Claim 2 wherein said associated memory is operable to store said circuit netlist as a data structure.

5. The IC simulation system as set forth in Claim 1 wherein said each one of said plurality of HDL modules is parameterized and specifies a logical operation.

6. The IC simulation system as set forth in Claim 5 further operable to selectively match, with directed acyclic graphs ("DAGs"), a logical operation of said HDL description with a parameterized HDL module that is capable of performing said logical operation.

7. The IC simulation system as set forth in Claim 1 wherein said timing-violation controller operates to not ignore ones of said selected timing violations sensed during simulation of said circuit as a function of ones of said defined behavioral relationships.

8. A method of operating an integrated circuit ("IC") simulation system comprising the steps of:

storing a plurality of Hardware Description Language ("HDL") modules in memory, each one of said plurality of HDL modules representative of a circuit element;

receiving a HDL description of a circuit to be simulated;

synthesizing a circuit netlist as a function of said received HDL circuit description and ones of said plurality of HDL modules, said circuit netlist defining behavioral relationships among associated ones of said ones of said plurality of HDL modules; and

associating a timing-violation controller with said circuit netlist, said timing-violation controller to ignore selected timing violations sensed during simulation of said circuit as a function of ones of said defined behavioral relationships.

9. The method of operating said IC simulation system as set forth in Claim 8 wherein said IC simulation system comprises a processor that is associated with said memory.

10. The method of operating said IC simulation system as set forth in Claim 9 further comprising the steps of:

storing an IC-design process program; and

executing said IC-design process program with said processor.

11. The method of operating said IC simulation system as set forth in Claim 9 further comprising the step of storing said circuit netlist as a data structure.

12. The method of operating said IC simulation system as set forth in Claim 8 wherein said each one of said plurality of HDL modules is parameterized and specifies a logical operation.

13. The method of operating said IC simulation system as set forth in Claim 12 further comprising the step of selectively matching, with directed acyclic graphs ("DAGs"), a logical operation of said HDL description with a parameterized HDL module that is capable of performing said logical operation.

14. The method of operating said IC simulation system as set forth in Claim 8 further comprising the step of operating said timing-violation controller to not ignore ones of said selected timing violations sensed during simulation of said circuit.

15. A computer readable memory that directs a computer to operate as an integrated circuit ("IC") simulation system, comprising:

a plurality of Hardware Description Language ("HDL") modules stored in said computer readable memory, each one of said plurality of HDL modules representative of a circuit element;

a HDL description of a circuit to be simulated stored in said computer readable memory;

executable instructions stored in said computer readable memory to synthesize a circuit netlist as a function of said HDL circuit description and ones of said plurality of HDL modules, said circuit netlist defining behavioral relationships among associated ones of said ones of said plurality of HDL modules; and

executable instructions stored in said computer readable memory to associate a timing-violation controller with said circuit netlist, said timing-violation controller to ignore selected timing violations sensed during simulation of said circuit as a function of ones of said defined behavioral relationships.

16. The computer readable memory as set forth in Claim 15 further comprising an IC-design process program stored in said computer readable memory.

17. The computer readable memory as set forth in Claim 15 wherein said circuit netlist is stored in said computer readable memory as a data structure.

18. The computer readable memory as set forth in Claim 15 wherein said each one of said plurality of HDL modules is parameterized and specifies a logical operation.

19. The computer readable memory as set forth in Claim 18 further comprising executable instructions stored in said computer readable memory to selectively match, with directed acyclic graphs ("DAGs"), a logical operation of said HDL description with a parameterized HDL module that is capable of performing said logical operation.

20. The computer readable memory as set forth in Claim 15 further comprising executable instructions stored in said computer readable memory to operate said timing-violation controller to not ignore ones of said selected timing violations sensed during simulation of said circuit.